NEPP Electronic Technology Workshop
June 23-26, 2015

Jet Propulsion Laboratory
California Institute of Technology

Zynq SoC Radiation Test Results and Plans for the Altera MAX10

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Acknowledgment:
This work was sponsored by:
NASA Office of Safety & Mission Assurance,
NASA Electronics Parts and Packaging Program

To be presented by Gregory R. Allen at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 23-26, 2015 and published on nepp.nasa.gov.

Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
Au	Gold
BRAM	Block Random Access Memory
CPLD	Complex Programmable Logic Device
DSP	Digital Signal Processor
DUT	Device Under Test
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
GEO	Geosynchronous Orbit
GSFC	Goddard Space Flight Center
JPL	Jet Propulsion Laboratory
Kr	Krypton
LBNL	Lawrence Berkeley National Laboratory
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LET_{TH}	Linear Energy Transfer Threshold
LUT	Look-up Table
MBE	Multi-Bit Event
MeV	Mega-Electron Volts
MMU	Memory Management Unit

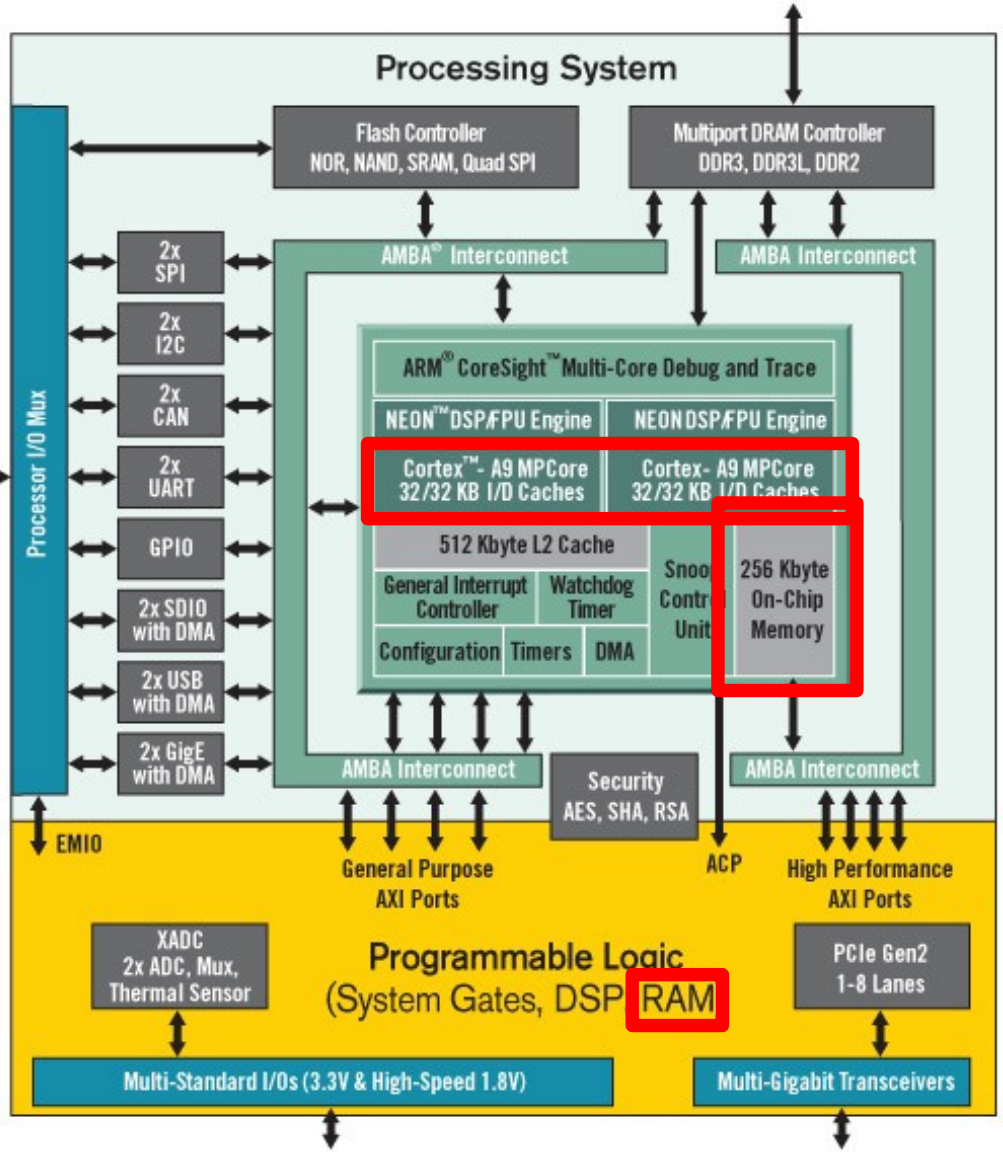
Acronym	Definition
NASA	National Aeronautics Space Agency
NEPP	NASA Electronic Parts and Packaging
nuc	Nucleon
OCM	On Chip Memory
P	Proton
PL	Programmable Logic
PLL	Phase Locked Loop
PS	Processing System
RISC	Reduced Instruction Set Computing
SBU	Single-Bit Upset
SEFI	Single Event Functional Interrupt
SEL	Single Event Latchup
SEU	Single Event Upset
SoC	System on a Chip
SRAM	Static Random Access Memory
TAM	Texas A&M
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TSMC	Taiwan Semiconductor Manufacturing Company
XADC	Xilinx Analog to Digital Converter
σ	Cross-Section

Xilinx Zynq Investigation Overview

- **Task Description—perform initial SEE characterization of Xilinx Zynq SoC FPGA.**
- **Primary focus last year was single-event latchup (SEL) screening, single-event upset (SEU) characterization of the configuration memory and block RAM, and processor cache and on-chip memory (OCM).**
- **General Test strategies based on *Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Radiation Testing* [Berg, 2012], and *SoC SEE Test Guideline Development* [Guertin].**

Xilinx Zynq Device Overview

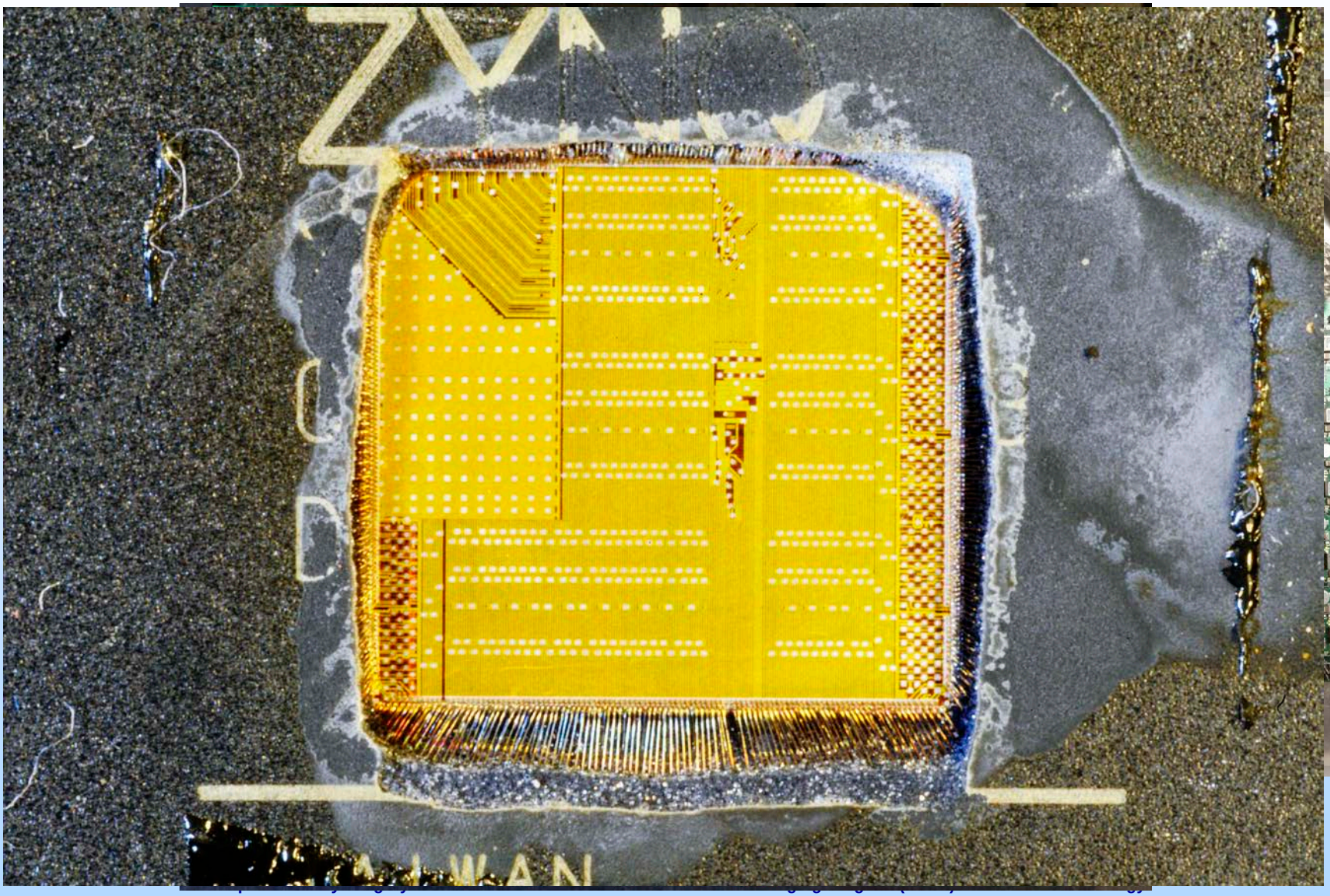
- System- ARM Cortex-A d 28nm Xilinx pr ngle device.
- PS conta , level 1 and 2 ca mory and peripher
- PL stand RAM (BRAM),
- See [Xili urce details.



FY14 Major Accomplishments

- Heavy ion test campaign at Lawrence Berkeley National Lab (LBNL) August 2014, and Texas A&M (TAM) April of 2014.
- Limited proton testing at LBNL.
- Observed SEL as observed by Berg et al and Lee et al
- Developed SEU cross-section vs. LET curve for configuration memory and BRAM.
- Acquired limited heavy ion and proton data on OCM.
- Attempted cache test with protons.

Test Methodology



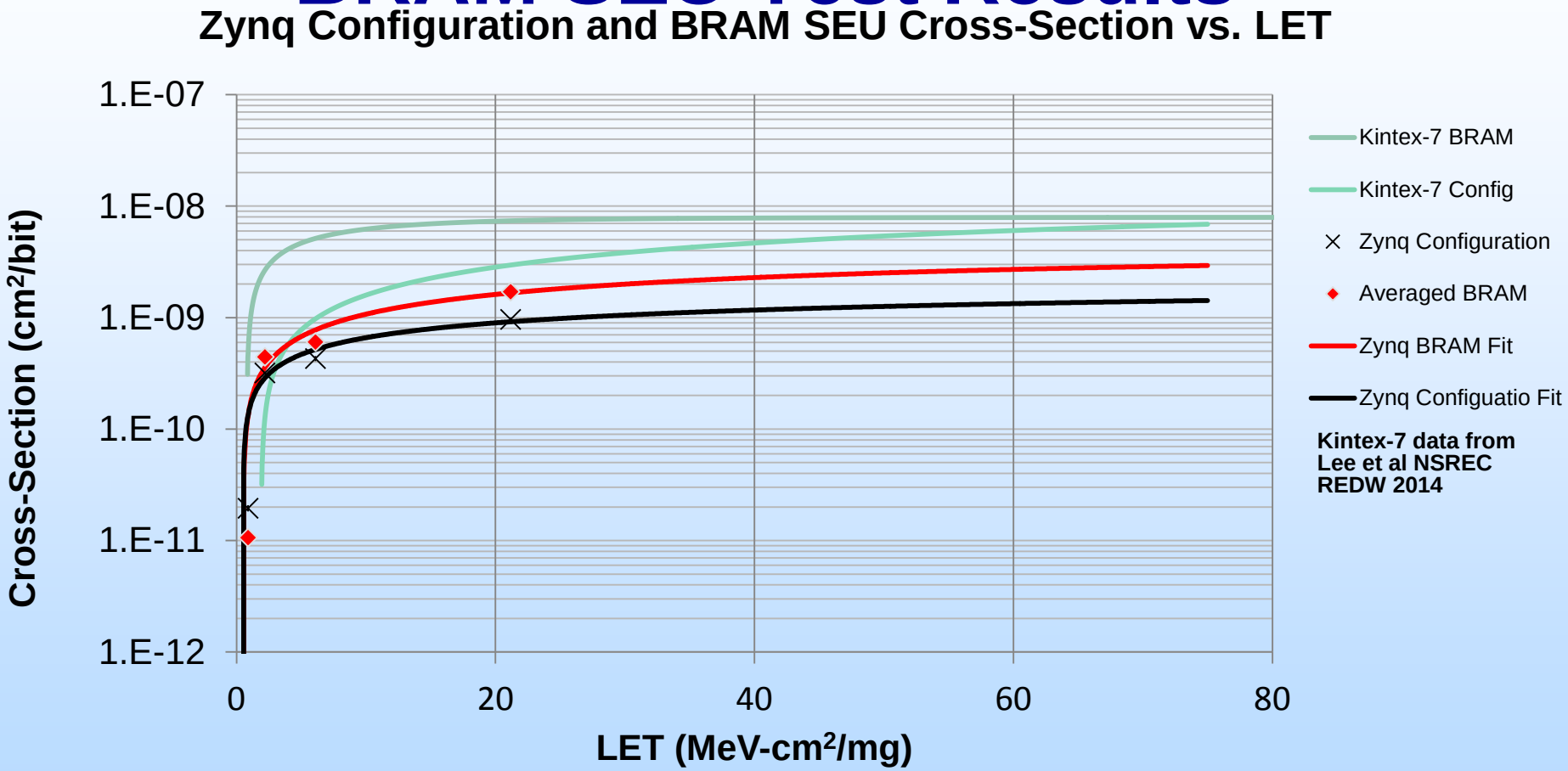
SEL Test Results

- **We observed similar SEL on 1.8V VCCAUX as GSFC, Sandia et al.**
- **Confirmed SEL by measuring increase in cross-section with temperature and removed SEL by reducing voltage (around 1.2V).**

Configuration Memory SEU Characterization Methodology - Zynq

- Power cycle (configure, verify design)
- Readback and save configuration bitstream with JTAG software
- Irradiate to known, set fluence
- Readback and save configuration bitstream for data analysis (custom script written to compare and count errors)
- Reconfigure device and repeat until statistics, LET_{TH} and saturation have been adequately measured.

7-Series Zynq Configuration Memory and BRAM SEU Test Results



- Note that the BRAM SEFI was observed as well.
  - 1's reset to 0's ~1024 at a time.

PS Test Methodology—OCM

- **The on-chip memory test was designed as a straightforward memory test with the following behavior.**
  - **Write a known pattern to the OCM (all OCM operations are from CPU0 only) – the pattern is 0x0000_0000 on all even passes and 0xffff_ffff on all odd passes.**
  - **Write a known pattern to about half of the ARM registers (both CPU0 and CPU1)**
  - **Wait for a given period of time (utilizing a machine language counter, not a timer)**
  - **Store the tested registers to a special area of memory.**
  - **Run a memory check for the expected pattern.**
  - **Store the OCM to a special area of memory.**
  - **Run a memory check for the expected pattern.**
  - **Note that for data analysis, the location in memory where a miss-compare is reported identifies if the error is from an ARM register or from the OCM.**

PS Test Methodology—Cache

- This program enables the L1 data cache, but disables the L1 instruction cache. It leaves the MMU in a flat configuration with no information about special memory handling (essentially it leaves the MMU as-is after power up – so it is disabled).
  - The software takes a 32 kB section memory (since the L1 data cache is 32 kB).
  - It writes the pattern 0xa5a5a5a5 to that memory region (0x2000 4-byte words) and then reads it back (thus regardless of cache mode, the pattern should be in the cache). Then the program waits a period of time.
  - Finally, it copies the memory region to another area (with the expectation of locking in any errors). And it then compares the new memory region to the expected values.

PS Test Results

Run #	Beam	LET/Energy	Fluence (#/cm^2)	Test Program	SBU	MBE	SBU σ (cm^2/bit)	MBU σ (cm^2/bit)
134	25 MeV/nuc Kr	24.3 MeV-cm^2/mg	1.01E+04	OCM	56	16	2.64E-09	7.55E-10
135	25 MeV/nuc Kr	24.3 MeV-cm^2/mg	7.39E+02	OCM	-	-	-	-
136	25 MeV/nuc Kr	24.3 MeV-cm^2/mg	9.43E+02	OCM	7	2	3.54E-09	1.01E-09
58	P	18 MeV	7.40E+08	OCM	7	0	4.51E-15	-
59	P	18 MeV	6.10E+09	OCM	103	0	8.05E-15	-
60	P	18 MeV	6.00E+09	OCM	107	0	8.50E-15	-
61	P	18 MeV	1.00E+10	Cache	0	0	<4.0E-16	-

- **The cache test did not yield any upsets.**
  - **It is unknown if parity is enabled on the L1 data cache.**
  - **It is unknown if the L1 cache is in write-through or write-back mode. And we are setting the bit that enables the data cache.**

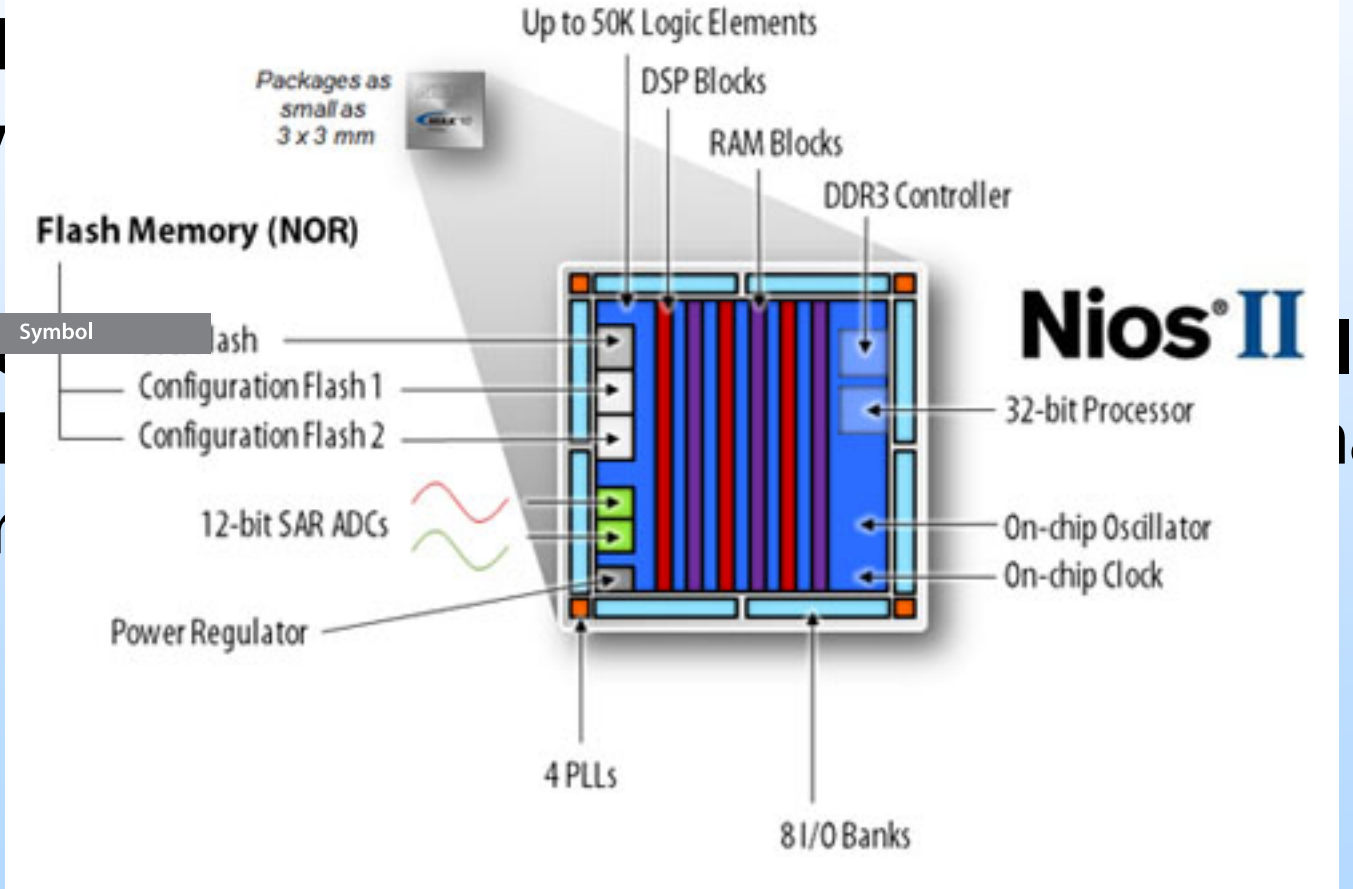
Altera MAX10 FPGA Task Overview

- **Task Description—perform initial SEL and TID characterization of Altera's CPLD Based MAX10 FPGA.**

- **General Test strategies based on *Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Radiation Testing* [Berg, 2012], and *SoC SEE Test Guideline Development* [Guertin].**

Altera MAX10 Architecture Overview

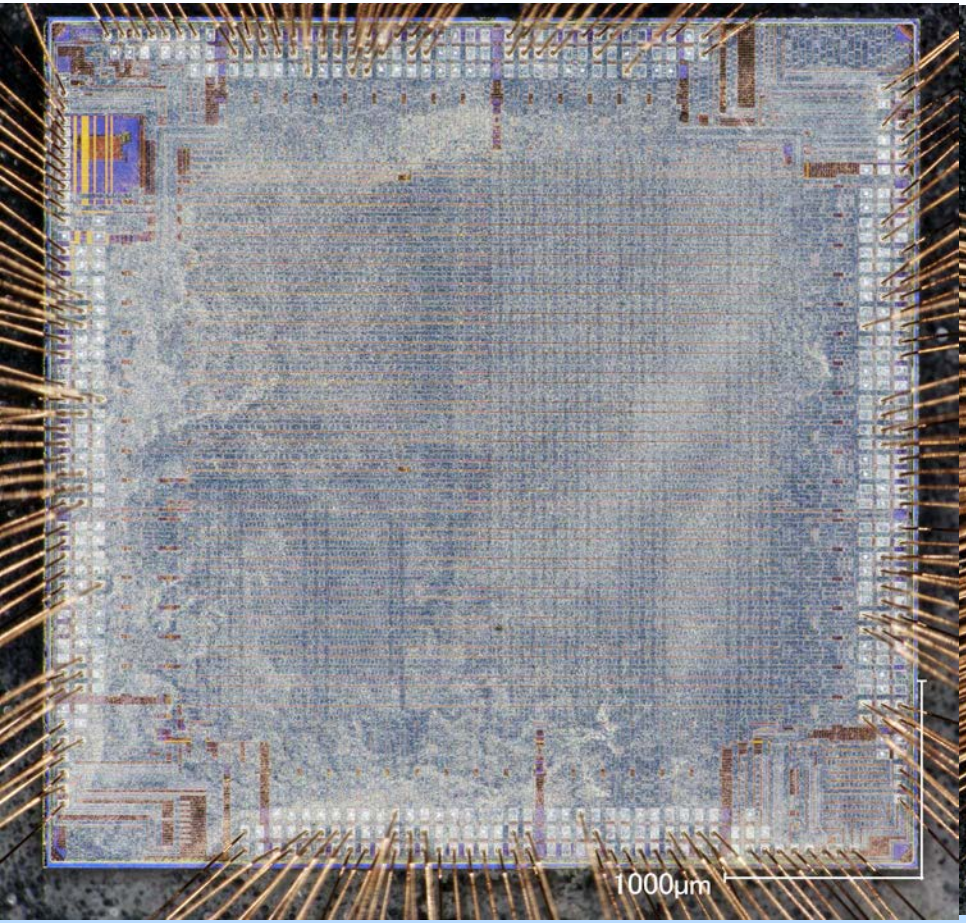
- Flash-based/SRAM-based FPGA based on TSM
- 1.2V devi
- Hav lash, 18x1 al mem

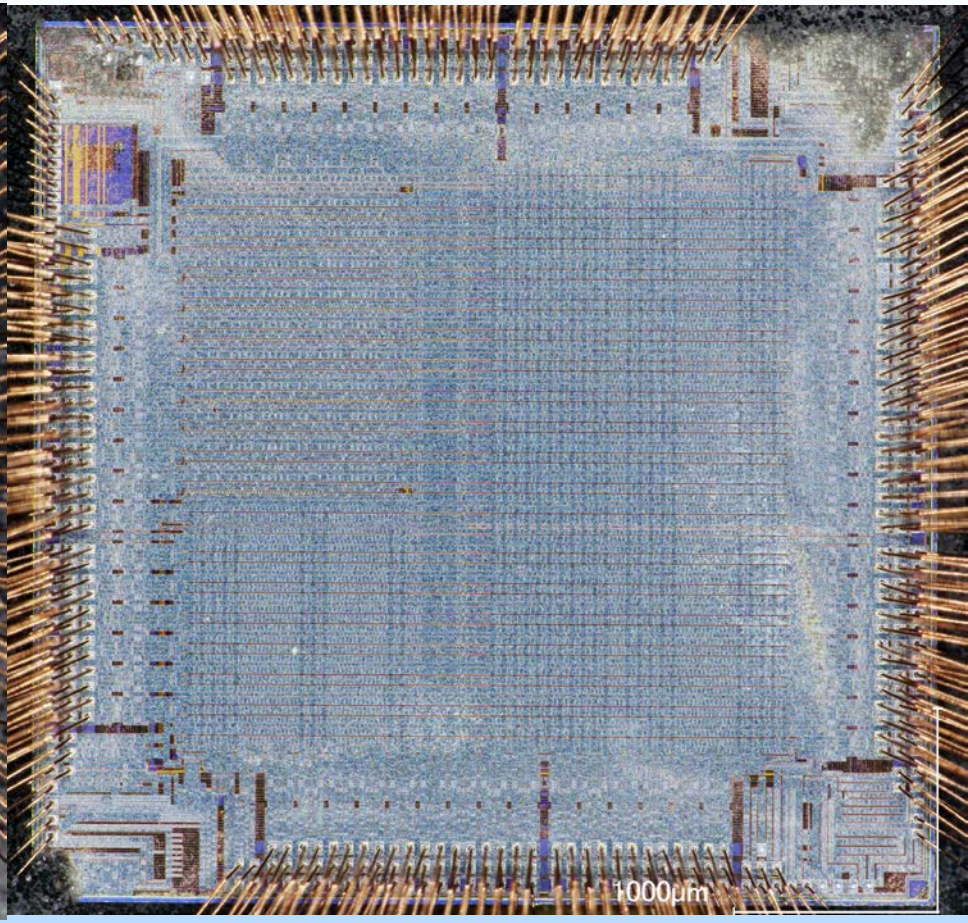


FY15 Major Accomplishments-MAX10

- **Procured two evaluation boards with 10M08SAE and 10M08DAF devices.**
  - **The SAE is single supply (VCC_ONE) and DAF is dual supply.**
- **Both boards are prepped and ready for SEL/TID testing.**
- **Completed initial TID testing on *VCC_ONE* version.**
- **Completed initial SEL test**

Test Boards



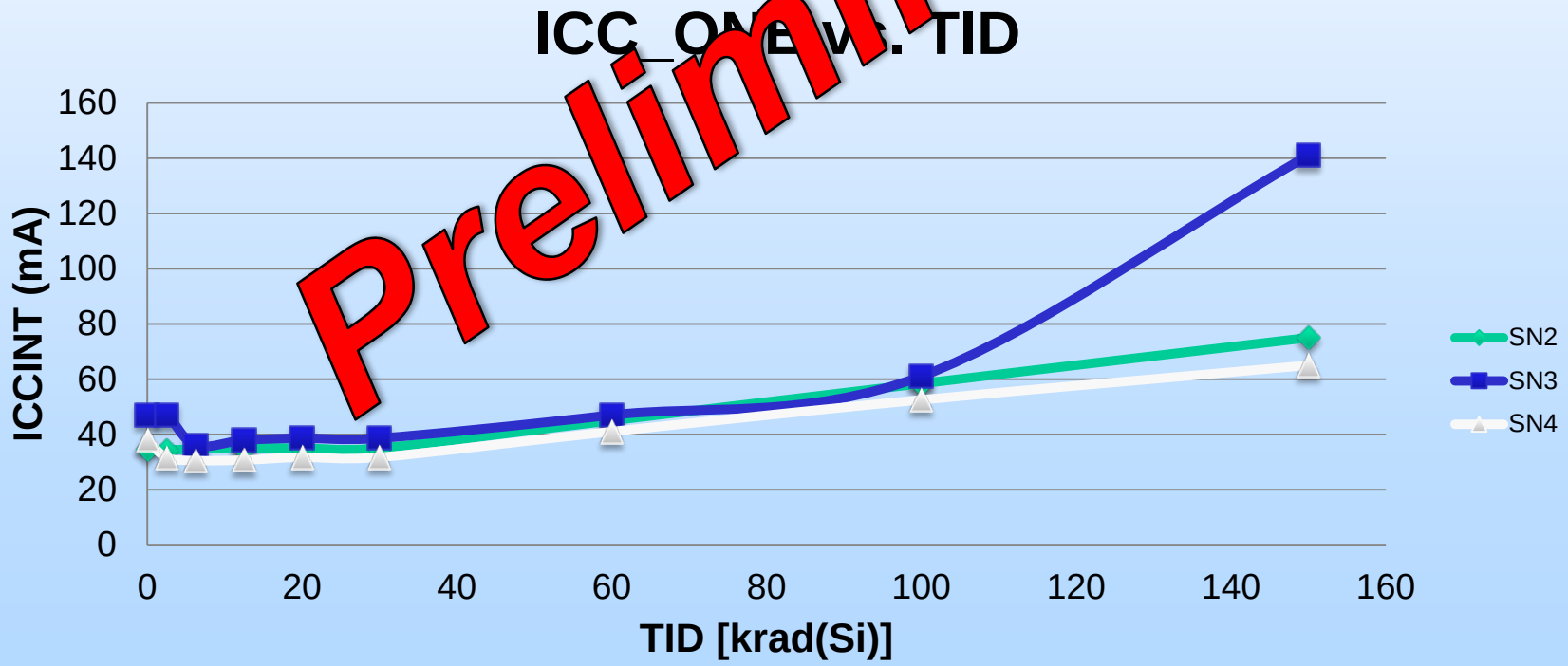


TID Test Plan

- **Phase 1 Test (Completed)**
  - **Initial test structures:**
    - **Simple shift register with combinatorial logic**
    - **Inverter chain**
  - **Single Supply (*VCC_ONE)***
  - **Biased, no-refresh mode**
- **Phase 2 Test (TBD)**
  - **Full processor implementation, ADC, PLL, etc.**
  - **Both FPGA types to be tested (single and dual supply).**
  - **Initially biased only, using both program refresh mode and no-refresh mode.**

Initial TID Results

- Tested at Co-60 facility at JPL.
- Tested MAX10 VCC_ONE device at 25 rad(Si)/second, biased, no-refresh.
- No timing degradation observed. Functional failure between 100 and 150 krad(Si).



SEL Test Plan

- **Basic SEL test (6 devices, three of each supply type), worst case bias, temperature, $1x10^7$ ions/cm^2 per DUT or 100 events**
- **Simple functional design**
- **Regulators removed from evaluation board and power directly supplied**
- **Custom software used to monitor and strip chart power, and automatically power cycle in the event of an SEL**

SEL Test Results

- Parts were tested for SEL at Texas A&M using 15 MeV/nuc Au and Ag beams, LET = 85.4 MeV-cm²/mg and 42.2 MeV-cm²/mg respectively.
- Parts tested with max bias at 85C.
- Both standard and *VCC_ONE* devices tested.
- Observed SEL on both devices
  - *3.3V VCC_ONE* 3.3V VCCA (supplies PLL regulator and ADC block)
  - *2.5V Dual Supply* VCCA (supplies analog ADC and PLL block)
- Saturated cross-section (85.4 MeV-cm²/mg) of $2.75X10^{-6} \pm 7.42x10^{-7}$ cm²/dev at 85C

Other SEL Test Notables

- **SEL only occurred during in a configured state**
  - **e.g. if the DUT was held in an unconfigured state, the effect was not observed.**
  - **Indicates ADC unpowered during un-configured state**
- **With Au, the configuration was knocked out instantly and required reprogramming on *VCC_ONE,* with the *Dual Supply* configuration remained intact.**
- **With Ag, both devices maintained configuration**
- **Opened power supply clamps and SEL maintained ~1.1A**
  - **Non-destructive event**

Conclusions

- **Lower budget missions (e.g. class D) will often select commercial devices**
- **Methodologies have been developed to ascertain a baseline SEE/TID susceptibility that scales with such missions budgets**
- **Much of the same historic reconfigurable FPGA mitigation approaches can be employed (TMR + scrubbing) as applicable.**